Stuck-at Fault Detection in Combinational Network Coefficients of the RMC with Fixed Polarity (Reed-Muller Coefficients)

Sharad Pratap Singh and Dr. B.B. Sagar

Abstract: The paper presents a new method for computing all $2^n$ canonical Reed-Muller forms (RMC forms) of a Boolean function and fixed polarity matrix method. The method constructs the coefficients directly and no matrix multiplication is needed. It is also usable for incompletely specified functions and for calculating a single RMC form. The method exhibits a high degree of parallelism. In the stuck-at model it is generally assume that a logic input or output is static or fixed to either logic ‘1’ (stuck-at one) or logic ‘0’ (stuck-at zero) and abbreviated as s-a-0 and s-a-1 respectively.

Keywords: Fault detection, Read Muller Coefficients, Boolean function.

I- INTRODUCTION

Digital systems are becoming increasingly complex and sophisticated development in LSI/VLSI technology which has allowed not only higher package density but also made it feasible to implement additional peripheral support devices that were earlier interconnected externally. In addition it permitted on-chip in corporation of novel advanced features such as self testing, supervisory and fail-safe etc. and hence simplified the task of design and maintenance of complex systems by reducing external interconnecting lines as also thought improved reliability. Many digital hardware building blocks such as Encoders/Decoders, ROM / Demux, ROMs, PLAs and ASICs are frequently use to generate multiple output combinational function to implement digital systems intended for various application areas such as DSP, Automation, Control and computer systems etc. The increasing use digital systems in all aspects of social, economic and industrial applications have necessitated developed.

II- METHOD FOR FAULT DETECTION:

Most commonly four methods are for used

1. Fault table method,
2. Boolean difference method
3. Path sensitization method and
4. D-algorithm

The advantage of this representation is the fact that the resulting circuit needs at most n inputs in contrast to up to $2n$ inputs in other cases. The second essential advantage is the fact that for each function represented in RMC form there exists circuit, which can be tested with maximum $3n + 4$ tests, most of them independent of the realized function [2]. It is easy to see that for a Boolean function with n variables there exist $2^n$ different RMC forms. Each of these forms can be characterized by $2^n$ Boolean values a, indicating the presence or the absence of a given product term.

The aim is now to find the RMC form with the least number of $a_i = 1$. Algorithms existing up to now build up a $2^n \times 2^n$ matrix, called polarity-matrix [7], where every coefficient $a_{ij}$ of each of the $2^n$ polarities is given. This polarity-matrix is constructed using matrix multiplication [3], which means that these algorithms belong to the class with complexity $AT^2 = O (16^n)$ [1] [3]

Method:

Definition: Let $T_n$ be a $2n \times 2n$ binary matrix. $T_n$ will recursively be defined as.

$$T_n = \begin{bmatrix} t_{n-1}^{n-1} & 0 \\ 0 & t_{n-1}^{n-1} \end{bmatrix}$$

And $T_0= [1]$.

It becomes apparent that the same matrix can be obtained by the $n$th Kronecker-power [12] of $T$. Definition:

Consider a Boolean function $f$ given as

$$[f] = [f', f'']$$

Where, $[f'] = [f_0, \ldots, f_{2^{n-1}-1}]$

And,

$$[f''] = [f_{2^{n-1}}, \ldots, f_{2^n}]$$

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Then \( B[f] \) is defined as
\[
B[f] = \begin{bmatrix}
B[f_0] & B[f']
\end{bmatrix}
\]
and \( B[fi] = fi \)

Let \( z^n \) be the \( n \)th Kronecker power of \( Z' = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \)

Then \( m[f] = B[f].2^n \)

\[
\begin{bmatrix}
P[000] & P[111] \\
P[110] & P[111]
\end{bmatrix} =
\begin{bmatrix}
\end{bmatrix}
\]

\[
\begin{array}{c|cccc}
w_1 & 3 & 4 & 3 & 3 & 5 & 2 & 3 \\
a_0 & 1 & 0 & 1 & 0 & 1 & 1 & 1 \\
a_1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\
a_2 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
a_3 & 0 & 0 & 0 & 1 & 1 & 1 \\
a_4 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\
a_5 & 1 & 1 & 0 & 0 & 1 & 1 & 0 \\
a_6 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\
a_7 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
w_2' & 4 & 5 & 3 & 4 & 7 & 4 & 5 \\
w_2 & 2 & 4 & 1 & 2 & 2 & 5 & 2 & 4 \\
w_0' & 8 & 11 & 9 & 9 & 7 & 13 & 7 & 10 \\
W=\sum w_i & 4 & 4 & 7 & 5 & 4 & 5 & 4 & 4
\end{array}
\]

That computation of the coefficients of the RMC forms off for a given polarity is possible without constructing the whole matrix \( P \). This can be advantageous in cases of lack of storage. The 3-output

Polynomials with polarity (000) are as follows:
\( f_0 = X_1 \oplus XOX1 \oplus X2 \oplus X0X1X2X3 \)
\( f_1 = X1 \oplus XOX1 \oplus X2 \oplus X0X1 \oplus XOX2X3 \)
\( f_2 = 1 \oplus X0 \oplus X0X2 \oplus X0X2 \oplus XOX1X3 \)

\[
P[f'] = P[f] = P[f''']
\]

\[
P[f'] = P[f'''] = P[f''']
\]

\[
P[f] = m[f]
\]

\[
\begin{array}{c|cccc}
\text{Inputs} & X_2 & X_1 & X_0 & f_1 & f_2 & f_0 \\
\hline
0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 & 1 & 1 \\
0 & 1 & 1 & 0 & 0 & 0 \\
1 & 0 & 0 & 1 & 1 & 1 \\
1 & 1 & 0 & 1 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 0 \\
\hline
\end{array}
\]

\[
\begin{array}{c|cccc}
\text{TABLE-1 The number of Ex-OR gates for the example} & X_2 & X_1 & X_0 & f_1 & f_2 & f_0 \\
\hline
a_0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \\
a_1 & 0 & 0 & 1 & 0 & 0 & 0 \\
a_2 & 1 & 0 & 1 & 0 & 1 & 1 & 1 \\
a_3 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\
a_4 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \\
a_5 & 0 & 0 & 1 & 1 & 0 & 1 & 1 \\
a_6 & 0 & 1 & 0 & 1 & 0 & 1 & 1 \\
a_7 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
w_0' & 4 & 4 & 7 & 5 & 4 & 5 & 4 & 4 \\
w_0' & 4 & 4 & 7 & 5 & 4 & 5 & 4 & 4
\end{array}
\]
To detect the single/multiple stuck-at faults and bridging faults in multiple output systems, it is proposed that above mentioned faults can be detected by verifying only one output function which contains all the input variables. If all the input variables do not appear in any of the output functions, then more than one function should be verified for fault detection. According to the proposal the faults in multiple output combinational circuits can be detected by considering the following cases.

Case I: When any one output function contains all input variables, then by testing only that function we can detect single/multiple stuck-at faults and single bridging fault of n input circuit by verifying at most n, RM coefficients. The saving of test sets and time is highest in this case.

Case II: When in all output functions some input variables do not appear than we have to test more than one functions so that all input variables may be involved in fault detection. In this case larger test sets and computations have been claimed than in the case-1.

Case III: When all the output functions are disjoint i.e., all functions have different input variables. Then all functions will be tested separately. It is the worst case in which largest test vectors and computations are required. It has been reported that any R.M. network with k output and n input (k ≤ 2n) requires at most 3n+5 test patterns to detect all single stuck-at faults and both AND and OR bridging faults which are detectable.

Concluding remarks:
A new method for the polarity matrix which is used for minimization of RMC forms of Boolean function is presented. It can be used for fully specified and incomplete specified functions.
In place of R. M. spectral coefficients techniques of fault detection, a more faster technique can be proposed to reduce further test sets and hardware overhead.
P[f] matrix may be generated with further less no. of iterations, by modifying generation process of it.

### Table 2. The No. of NOT, AND & Ex-OR gates for the example

We see that the polarity (011) requires 4 Ex-Or gates for realization of the 3-output functions with regard to the common terms which is minimum than other polarity, hence polarity, hence polarity 3(011) is the optimum one. The number of input NOT gates, output NOT gates and EX-OR gates.

<table>
<thead>
<tr>
<th>Polarity</th>
<th>000</th>
<th>001</th>
<th>010</th>
<th>011</th>
<th>100</th>
<th>101</th>
<th>110</th>
<th>111</th>
</tr>
</thead>
<tbody>
<tr>
<td>W_0</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>5</td>
<td>2</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>W_1</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>W_2</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>W</td>
<td>8</td>
<td>11</td>
<td>9</td>
<td>9</td>
<td>7</td>
<td>13</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>W_{E2}</td>
<td>0</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>W_{E4}</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N_s</td>
<td>2</td>
<td>5</td>
<td>4</td>
<td>5</td>
<td>1</td>
<td>7</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>N_s_2</td>
<td>6</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
</tbody>
</table>

Table: 3-output function

### Table 3: 3-output function

w0 3 3 5 4 2 3 3 3
a0 0 0 1 0 1 1 1 0
a1 0 0 1 1 1 1 1 1
a2 1 0 1 0 1 1 1 1
a3 1 1 1 1 0 0 0 0
a4 0 1 0 0 1 0 0 0
a5 1 1 0 1 1 1 1 0
a6 0 1 0 1 0 1 0 1
a7 1 1 1 1 1 1 1 1

TABLE 2. The No. of NOT, AND & Ex-OR gates for the example
REFERENCES


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