Design and Control of Asymmetrical Multi-level Inverter with Minimum Switching and Losses

Active Voltage Balance

M. siva sankar, Rajesh Reddy Duvvuru, RajaReddy Duvvuru

Abstract—Hybrid cascade multilevel inverters combine semi-conductor devices of different voltage ratings and technologies, which theoretically allow high efficiency to be achieved. They allow one to design single- and three-phase inverters that can be operated either with staircase or with PWM. The proposed modular concepts define new configurations that increase the flexibility for choosing suitable switches. The concept of energy balance domain has been introduced to characterize the achievable operating modes and power factor. The proposed supply simplification is best suited for applications that do not require high power factor over the full inverter magnitude. The bottlenecks of these topologies are, however, the need for isolated supplies for the cells and the lack of modularity. This paper focuses on the design and control of high-resolution, high-efficiency multi-level inverters with simplified dc power supplies. It introduces several rules for systematically designing the dc voltages of the cells, for which all unsupplied capacitor voltages can be regulated.

Six classes of inverters are obtained covering single- and three-phase, staircase and pulsewidth-modulated (PWM) inverters. New configurations of hybrid cascade multilevel inverters are obtained for each class. A double modulation strategy with two different frequencies is proposed that allows switching losses of PWM in-verters to be reduced. Decoupled mechanisms are proposed for the total and internal energy balances. It is shown how to make the design robust by taking into account conversion losses and large dc-voltage imbalances in the design and control. An analysis of the maximum voltage utilization and efficiency of the resulting configurations is carried out. The effectiveness of the novel concepts is validated experimentally for two of the proposed topologies.

KeyWords—AC–DC power converters, asymmetrical multi-level inverters, cascade multilevel inverters, hybrid multilevel inverters, multilevel inverters, multilevel topologies.

INTRODUCTION

Multi level inverters have attracted interest for increasing the operating voltage of power conversion devices far beyond the blocking voltage of single switching devices and also for reducing the distortion of the waveforms applied to the load. Among the available topologies, cascade multilevel inverters [2] are conceptually the simplest as they combine standard H-bridge inverters in series. Hybrid asymmetrical cascade multilevel inverters, however, present many challenges as they combine cells of different voltage ratings [5], [6], different topologies, or even combine switch converters pabilities and low relative conduction losses, with fast switches, featuring low switching losses at obtaining a hybrid inverter with better equivalent switches that would feature fast switching capability, low conduction losses, and low switching losses. By operating the high-voltage cells at reduced switching frequency, far below the pulsewidth modulation (PWM) frequency, performing the PWM only with the low-voltage cells, the conversion losses of the inverter alone can indeed be reduced. The main property supporting this result is that the transitions between most pairs of levels involve only the transition of the low-voltage cell. This cannot, however, be achieved for all topologies for all operating points. By designing and controlling the inverter appropriately, it is, however, possible to modulate all pairs of adjacent levels by switching only the low-voltage cells [6], [9], [10]. It has to be noted that the ideas formerly de-veloped in [11] for quasilinear amplifiers are conceptually very similar and mathematically yield exactly the same design and control strategies. The concepts for obtaining reduced switch-ing losses have been optimized and generalized for single-phase inverters by the introduction of optimized transition graphs in the switching-state space [9] and for three-phase inverters by introducing the concept of modulation domain [10].

The bottlenecks that still prevent the deployment of these topologies for industry applications are as follows:

1) the need for isolated supplies for all cells, which increases the complexity, cost, and losses of the inverter;
2) the difficulty of designing and controlling topologies with simplified supplies. This increases the complexity of the control and reduces the maximum voltage utilization of the inverter. As it is not possible to use the full inverter voltage, it is necessary to augment the blocking voltage capability of the inverter, which results in augmented cost and reduced energy efficiency;
3) the lack of modularity.

The supply issues have attracted the attention of many re-searchers. Rech and Pinheiro derived design rules for canceling passively the circulation of power between the cells, in order to allow the supply with only rectifiers [2]. Mariethoz and Rufer proposed an efficient multisource dc–dc converter to reduce supply losses [3]. Du et al. investigated how to apply programmed PWM in the context of partially supplied inverter [5]. Lu and Corzine proposed the use of a topology where a motor load serves as isolation between the dc links of two NPC inverters [4]. Steimer and Manjrekar proposed a topology that combines three-phase neutral point clamped (NPC) with unsupplied filtering floating H-bridge cells [7].

Veenstra and Rufer investigated active charging and balancing strategies for this topology based on the control of common-mode harmonics [8]. The two main innovations in [7], [8], [14], [16] are the use of a three-phase inverter with a common dc-link as high-voltage cell, and the use of the
low-voltage cell only as filtering devices, such that they do not require any additional supply.

This paper unifies and completes these works by establishing a theory for systematically designing hybrid cascaded multilevel inverters with simplified dc power supply and low losses. It derives a set of design rules that defines six classes of inverters for which an active balance and an efficient modulation can be applied. Single-phase and three-phase topologies exhibit different properties. Inverters with staircase (low frequency) modulation and inverters with PWM (high frequency) are designed in different ways. For the latter, the design rules are extended to take into account losses and voltage imbalances to obtain robust solutions.

Fig. 1. Investigated single-phase inverter topologies combine cells with different supply voltages and switch devices voltages (a) and technologies (b). (a) General single-phase topology. (b) Asymmetrical cascade inverter..

1. MULTILEVEL INVERTER MODEL

The design and control of single- and three-phase hybrid cascaded multilevel inverter topologies for which at least two rows have different voltage ratings and switch technologies and for which only the row with the highest voltage is supplied. Examples of such topologies are represented in Figs. 1 and 2. For the three-phase topologies, we only consider structures that combine a supplied three-phase cell with unsupplied single-phase cells as for the topologies represented in Fig. 2.

The regulation of the voltages of all unsupplied capacitors in these topologies is complex for two main reasons: First, the energy is stored in capacitors that are distributed both over the phases of the inverter and over the cells within a phase. Second, due to the asymmetry of the dc-voltages, the cells of different voltage ratings need to be coordinated to generate the desired output voltage.

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There are two necessary conditions for regulating the dc-voltages of all unsupplied capacitors to their reference value, while tracking the reference voltage and current trajectories.

1) The total low-voltage cell energy can be regulated only if the low-voltage cell does not provide any active power on average. The high-voltage cell must, therefore, provide the total power on average, while the low-voltage cell can only provide reactive, harmonic, and transient powers.

The dc-voltages can be regulated only if the distribution of energy within the low-voltage cell over its phases and rows can be modified, while preserving the inverter target output voltage.

Fig. 2. Investigated three-phase inverter topologies combine one three-phase cell with single-phase cells and thus feature a single dc supply. (a) General three-phase topology. (b) Hybrid inverter with two-level three-phase inverter and H-bridges.

The first necessary condition for balancing the total low-voltage cell energy requires the high- and low-voltage cells to operate in one of the modes below.

1) For space-vector references smaller than the high-voltage cell maximum magnitude, the high-voltage cell is able to provide the full-voltage on average; the low-voltage cell only needs to provide harmonic filtering that allows it to precisely generate the reference [see Fig. 3(a)].

2) For space-vector references exceeding the high-voltage cell maximum magnitude, the maximum power factor can be reached by keeping the high-voltage cell contribution parallel to the current, while the low-voltage cell provides a voltage contribution
orthogonal to the space-vector current on average, in order to increase the inverter achievable voltage magnitude [see Fig. 3(b)].

3) The maximum magnitude can be reached by contributing to the orthogonal component of the voltage with both high-voltage and low-voltage cells: the achievable power factor is lowest in this mode [see Fig. 3(c)].

The analysis of these operating modes leads to two definitions that will be useful through our developments.

1) Energy balance domain: This is the set of voltage vectors, represented in light gray in Fig. 3, that can be reached by the high-voltage cell alone on average. There is no or little restriction on the current waveform for trajectories fully belonging to this set. If the converter were only operated in this region, the capacitor could be very small, ideally close to zero. For steady-state operation, a larger set can be defined that corresponds to the set of voltages for which any power factor can be achieved, that is represented in Fig. 3 by augmenting the previous set with the dark gray area.

2) Limited energy balance domain: This is the set of voltages vectors that can be reached by the converter but that are not in the energy balance domain, represented by the area below the black bold dash curve in Fig. 3. The current trajectory for these vectors must be cyclic and fulfills some restrictions. In steady-state operation, this corresponds to a restriction on the achievable power factor and magnitude. In this domain, the ability to exchange power between phases is very limited. The capacitors, therefore, need to be sufficiently large to ensure that the voltage ripple remains small while storing the energy required for providing reactive and harmonic power over each cycle. 

To balance the low-voltage cell total energy, it is sufficient to operate the converter in one of the three modes described previously in Section II-C. To achieve this, while ensuring that the target space vector is generated at the output of the converter, it is necessary to follow the design rules that will be derived in this section. The keys underlying total and internal balance, while guaranteeing the tracking of the reference level trajectory, independently of the current trajectory, are the design and exploitation of redundant space vectors to adjust the cell power flows. To simplify the explanations, we will consider two series-connected cells, without loss of generality, since we can repeat the reasoning by associating two series-connected cells in a larger cell that would become the new low-voltage cell in the reasoning.

Each cell $c_{ij}$ is characterized by its number of levels $N_i$ and its nominal voltage step between two adjacent levels $V_i$. For the design condition to obtain balance of the low-voltage cell is derived by investigating the controllability of the direct-space of the low-voltage cell contribution. In Fig. 6(a)–(d), the different options for synthesizing a target space vector $V_o$ are investigated. If the space vectors strictly inside this triangle can be generated in three different ways, each activating one of the three adjacent space vectors of the high-voltage cell, as illustrated in Fig. 7(a)–(c), then it is clear that the modulated low.

II. DESIGN CONDITIONS FOR ENERGY BALANCE

Since the output voltage must not be affected by the regulation of the dc voltages, the manipulation of the component orthogonal to the current in the $\alpha\beta$ plane needs to be done in a complementary way on the high- and low-voltage cells. Operating in a complementary way with the high-voltage cell means that this can be done only slowly in an average sense. Moreover, compensation in the $\alpha\beta$ plane decreases the available magnitude of the high-voltage cell. It cannot be done for magnitudes close to the maximum achievable magnitude in the energy balance domain. For these reasons, balance through the common mode is preferred and is the only applied principle for correcting phase imbalance in Section VIII, but additional compensation of im-balance with compensation in the $\alpha\beta$ plane can be envisaged to improve the overall balance, for instance by reducing the ripple for known trajectories. If the space vectors strictly inside this triangle can be generated in different three ways, each activating one of the three adjacent space vectors of the high-voltage cell, as illustrated in Fig. 7(a)–(c), then it is clear that the modulated low-voltage cell contribution built using (6) can take any direction. The space vectors that are on the corners of the area do not need to be redundant since the contribution of the low-voltage cell to these is zero for these. The other space vectors on the side of the area need to have two realizations: this is where the contribution of the low-voltage cell needs to be the largest, which yields the worst case illustrated in Fig. 7(d). The associated design condition derived based on the worst case constraints the high-voltage. PWM operation of different voltage vectors to smoothly control the output voltage can readily be superimposed using the same balancing concepts, but it may result in excessive switching losses due to the operation of the high-voltage cells at the PWM
frequency. Design conditions to operate the high-voltage cells at low switching frequency have already been derived for single-[9] and for three-phase inverters [10], but without considering energy balance. This section derives design rules that allow the low-voltage cell energy balance and the optimal operation of the high-voltage cell at low switching frequency.

IV. PERFORMANCE EVALUATION

1) Design of the Inverter Configuration: The design rules that have been derived in the previous sections are summarized in Table I. The rules of Section IV are omitted since they are equivalent to the robust rules derived in Section VI when $n = 0$. As there are infinitely many inverter configurations fulfilling conditions (26) of Table I, some additional design constraints are imposed.

2) Selection of the Semiconductor Devices: One of the main differences with cascade symmetrical multilevel inverter topologies is that the switching frequency depends on the cell voltage rating, i.e., on its row index $i$. For the low-voltage cells, the design is, however, very similar to other PWM voltage-source inverters. The best tradeoff between switching losses, conduction losses, and possibly other criteria such as cost has to be found. For the high-voltage cells, the fact that they inherently switch slowly mostly affects the selection of the switch type: as their switching losses only marginally affect the overall losses, switching devices with low ratio between conduction losses and switching losses are preferred. Since the thermal energy to be transferred out of the high-voltage cells through the cooling system will be smaller than for other topologies, this allows a slight reduction of the cooling and/or current rating of the cell. The ratio on the left-hand side of the inequality depends on the selected configuration. Its upper limit on the right-hand side of the inequality only depends on the number of levels of the high-voltage cell. It is attained when the upper limit of condition (26d) is attained. The main interpretation of (26) is that the voltages for which the inverter energy can be balanced without restriction on the power factor increase with and only depends on the number of levels of the high-voltage cell.

V. RESULTS

Hardware Prototype: A modular hybrid cascaded multi-level inverter prototype has been built to validate the proposed concepts. Each module implements a three-phase cell made with three H-bridge power modules. The modules were assembled using different types of power switching devices available in the same package to test some of the topologies discussed in Section II.

Software prototype: The control algorithms were implemented in C using a DSP board [21] with a DSP from Analog Device (Sharc ADSP 21062 40 MHz). The multilevel PWM is implemented using an on-board FPGA from Xilinx (Spartan XCS-40). The control algorithms were tested on an induction motor drive. The drive stator voltage reference was obtained applying the field-oriented model predictive torque controller presented in [22].

the performance of the three-phase PWM inverter configurations (a) of Table II is evaluated. This topology is as
A torque profile is applied to the drive in Fig. 15. Fig. 15 demonstrates good dynamic operation during transients as well as the absence of distortion of the waveforms in steady state.

VI. CONCLUSION

Six rules for designing hybrid cascaded multilevel inverters with simplified supply and low switching losses have been derived. These design rules constrain the ratio between the dc volt-ages of the supplied cells and the dc voltages of the unsupplied cells. They allow one to design single- and three-phase inverters that can be operated either with staircase or with PWM. The proposed modular concepts define new configurations that in-crease the flexibility for choosing suitable switches. The concept of energy balance domain has been introduced to characterize the achievable operating modes and power factor. The proposed supply simplification is best suited for applications that do not require high power factor over the full inverter magnitude. For these, the switching devices can be optimally used, which results in a very high energy efficiency and very high number of levels. The internal balance of the cells over the phases and within the phase can be decoupled from the total energy regulation. The former is best done by controlling the common-mode voltage of the low-voltage cell. Applying the proposed voltage regulation and double modulation concepts, the solution is suitable for high dynamic performance.

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1. M. siva sankar received the B.Tech in electrical and electronics engineering from NECG, JNTUA University, Andhra Pradesh, India in 2012, where he is Presently Pursuing the M.Tech Degree from JNTUA University, Andhra Pradesh. He is research interests power converters.

2. Rajesh Reddy Duvvuru received the B.Tech in electrical and electronics engineering from JNTUA University, Andhra Pradesh, India in 2009, the M.Tech Degree from JNTUA University, Andhra Pradesh, India in 2011, where he is Presently Pursuing the Ph.D. degree in electrical engineering at The university Jodhapur, India. He is currently working as Asst.Prof at NECG, AP. He is research interests include power converters and control of Renewable Energy Power systems.

3. RajaReddy Duvvuru received the B.Tech in electrical and electronics engineering from JNTUA University, Andhra Pradesh, India in 2009, the M.Tech Degree from JNTUA University, Andhra Pradesh, India in 2011, where he is Presently Pursuing the Ph.D. degree in electrical engineering at JNTUA University, Andhra Pradesh, India. He is currently working as Teaching Asst at JNTUACEP, AP. He is research interests include Power systems, FACTS Devices.